--Sealing portion 50 is formed so as to effect sealing by molded resin 48 so as to cover first element 14, rearrangement sheet 26, second element 16, first wires 46, first relay wires 42 and second relay wires 44 on the upper surface of substrate 12.--

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IN THE CLAIMS:

Please cancel claims 16-20 without prejudice or disclaimer to the subject matter recited therein.

Please amend the claims as follows:

1. (Amended) A rearrangement sheet comprising an insulating sheet, said insulating sheet having an element mounting region defined thereon; and

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conductive metallic patterns formed on the insulating sheet so as to surround, and not extend into, the element mounting region.

5. (Amended) The rearrangement sheet according to claim 4, wherein said conductive metallic patterns comprise a laminated pattern of an underlying plated pattern formed on an upper surface of the insulating sheet and a conductive metal plated pattern formed on this underlying plated pattern.

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6. (Amended) The rearrangement sheet according to claim 1, wherein an insulating adhesive sheet is provided in the element mounting region.

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8. (Amended) A semiconductor device comprising:

a substrate;

a first element provided with a plurality of first bonding pads, and being disposed in a first element formation region on an upper surface of the substrate;

a second element provided with a plurality of second bonding pads, the second element being disposed over an upper side of the first element;

a plurality of bonding posts provided on the upper surface of said substrate, and outside so as to surround the first element formation region;

first wires that connect respective ones of the bonding posts with respective ones of said first bonding pads; and

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a rearrangement sheet provided with an insulating sheet, and a plurality of conductive metallic patterns that are formed on the insulating sheet, the rearrangement sheet being provided between said first element and said second element;

wherein said conductive metallic patterns are formed in a region exposed from said second element, so that the conductive metallic patterns surround, and do not extend under, the second element, said conductive metallic patterns each including a first portion that can be reached by a straight line extending from another respective one of the bonding posts for a second pad connection, without contacting or crossing said first bonding pads, and a second portion, capable of wire bonding with a respective one of the second bonding pads, thereby coupling the another respective one of the bonding post to the second bonding pad;

the first portions and the respective another ones of the bonding posts being connected by first relay wires; and

said second portion and said respective ones of the second bonding pads being connected by second relay wires.

9. (Amended) The semiconductor device according to claim 8, wherein said conductive metallic patterns include an underlying plated pattern formed on an upper surface of said insulating sheet, and a conductive metal plated pattern formed on the underlying plated pattern.

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10. (Amended) The semiconductor device according to claim 8, wherein said conductive metallic patterns are metallic wiring patterns formed on an upper surface of said insulating sheet.

11. (Amended) The semiconductor device according to claim 8, wherein said conductive metallic patterns comprise a metallic wiring pattern formed on an upper surface of said insulating sheet and conductive metal plated patterns provided on the metallic wiring patterns including the first portion and including the second portion.

12. (Amended) A semiconductor device, comprising:

a semiconductor element having a plurality of bonding pads formed on an upper surface thereof;

a rearrangement sheet comprising an insulating sheet and conductive metallic patterns electrically connected with said bonding pads, stuck onto the upper surface of

the semiconductor element other than in a region where the bonding pads are formed so as to be surrounded by the bonding pads; and

a sealed portion that seals the upper surface of said semiconductor element so as to cover said rearrangement sheet;

wherein said conductive metallic patterns comprise rearrangement posts of a same number as said bonding pads, wire connection portions of the same number as the bonding pads, the rearrangement posts and the wire connection portions being arranged so that the rearrangement posts are surrounded by the wire connection portions, and rewiring leads that connect said rearrangement posts and said wire connection portions;

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said wire connection portions and said bonding pads are connected by metallic wires,

conductive posts are formed on an upper surface of said rearrangement posts; and

part of the conductive posts is exposed from said sealed portion.

15. (Amended) The semiconductor device according to claim 12, wherein, of said conductive metallic patterns, said rearrangement posts and said rewiring leads are constituted by first metallic wiring patterns; and

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said wire connection portions are constituted by second metallic wiring patterns and conductive metal plated patterns formed on the second metallic wiring patterns.